

FIG. 2A

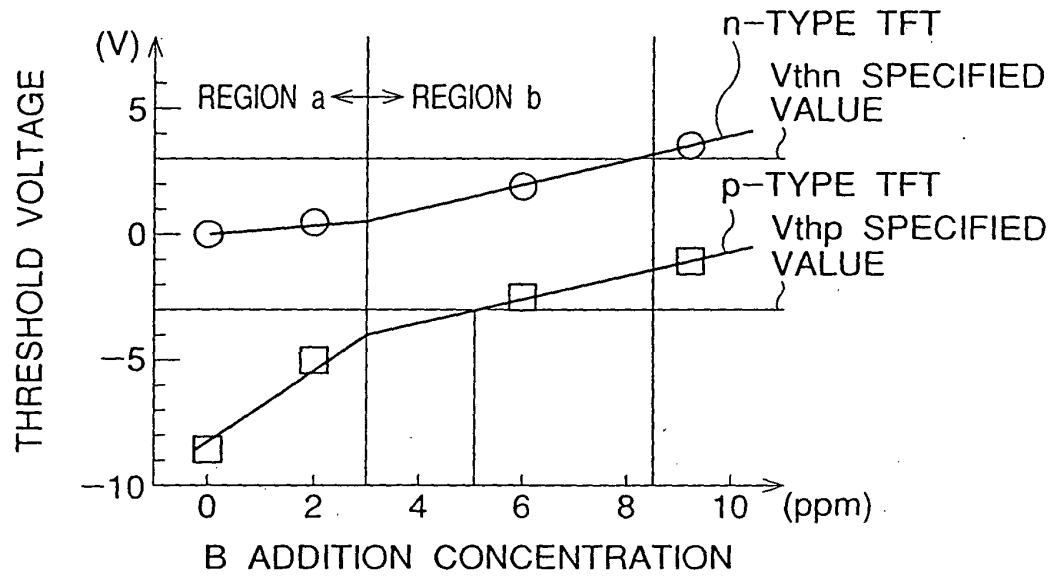


FIG. 2B

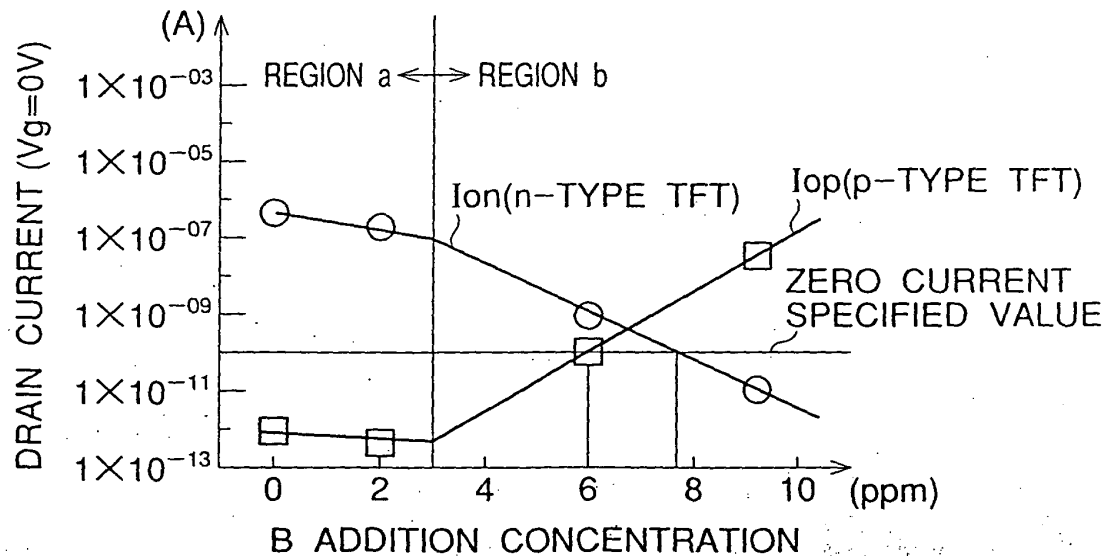


FIG. 3A

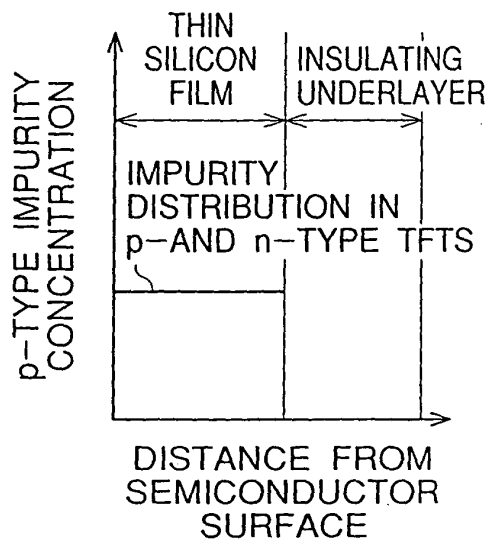


FIG. 3B

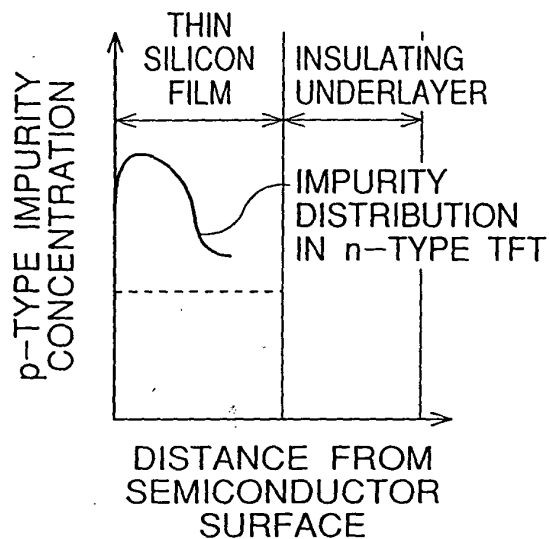


FIG. 3C

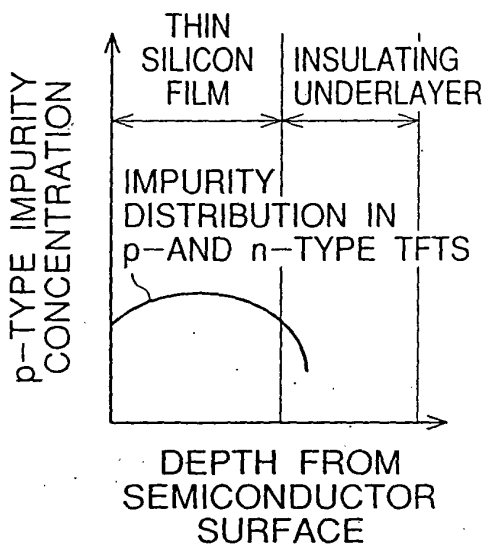


FIG. 3D

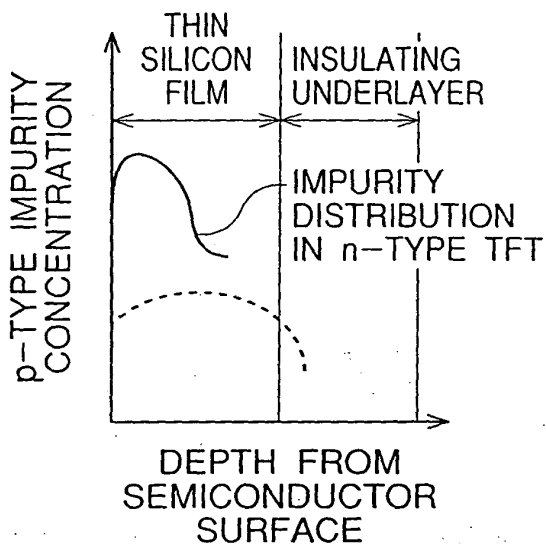


FIG. 4A

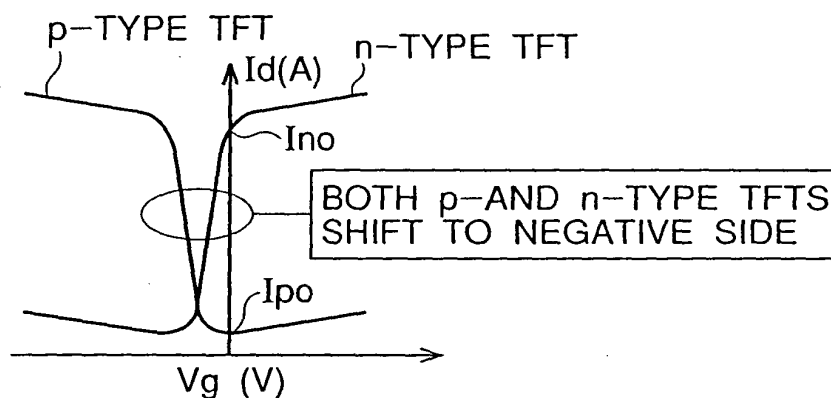


FIG. 4B

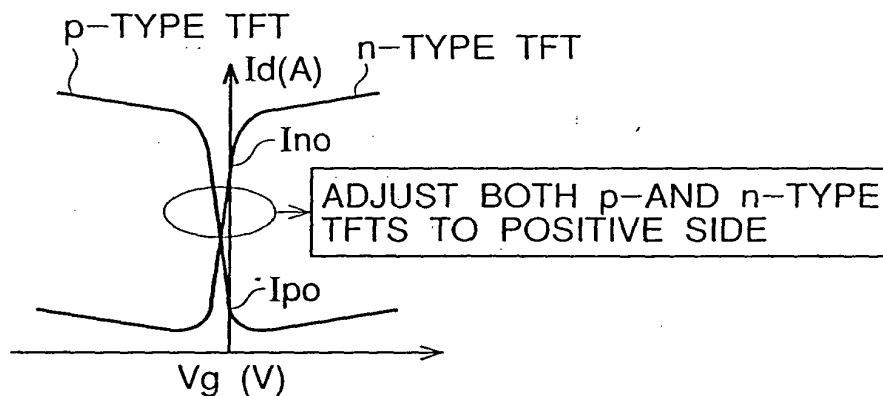


FIG. 4C

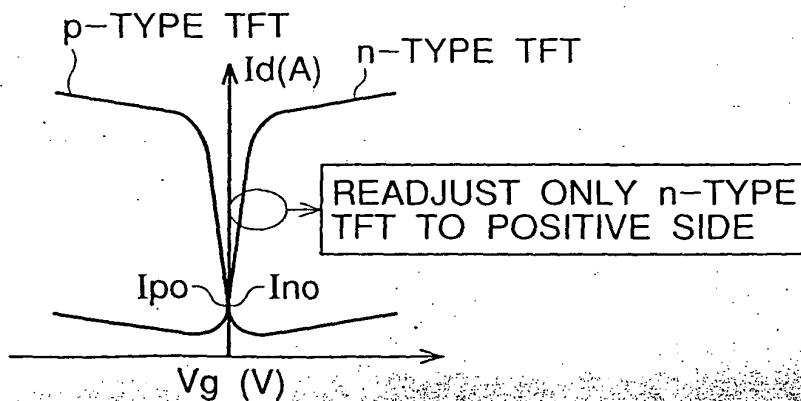


FIG. 5A

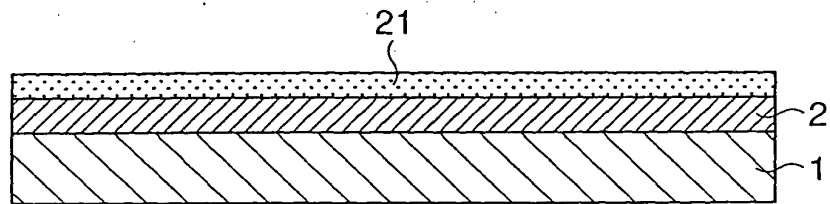


FIG. 5B

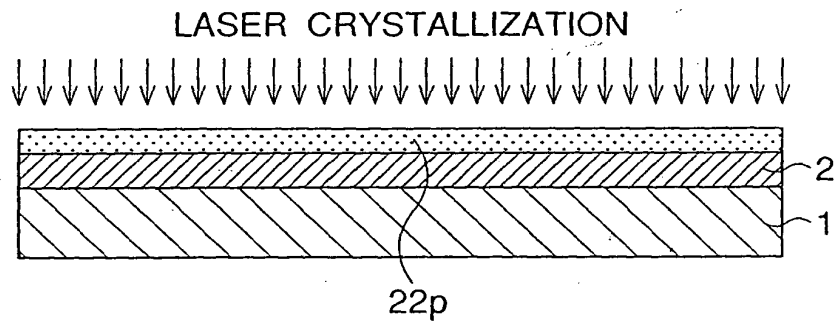


FIG. 5C

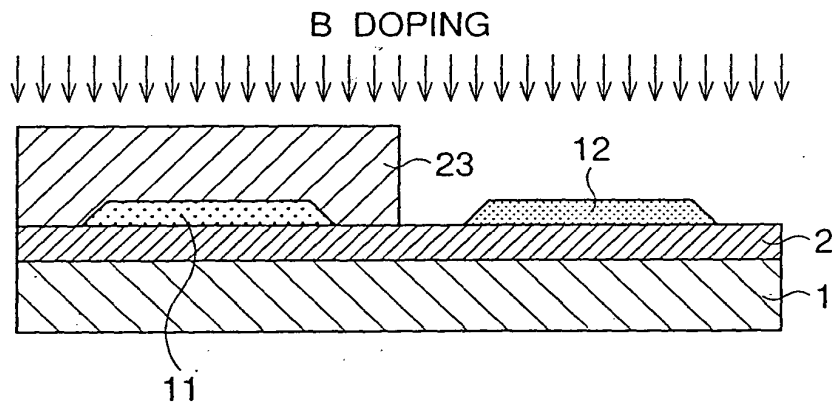


FIG. 5D

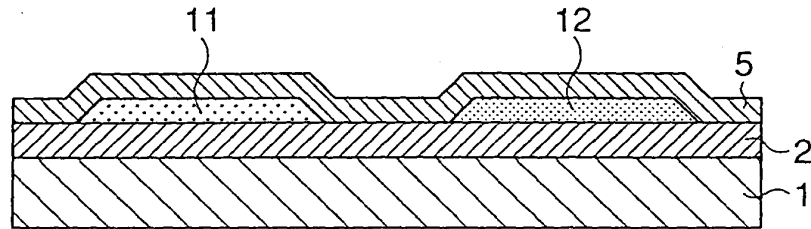


FIG. 5E

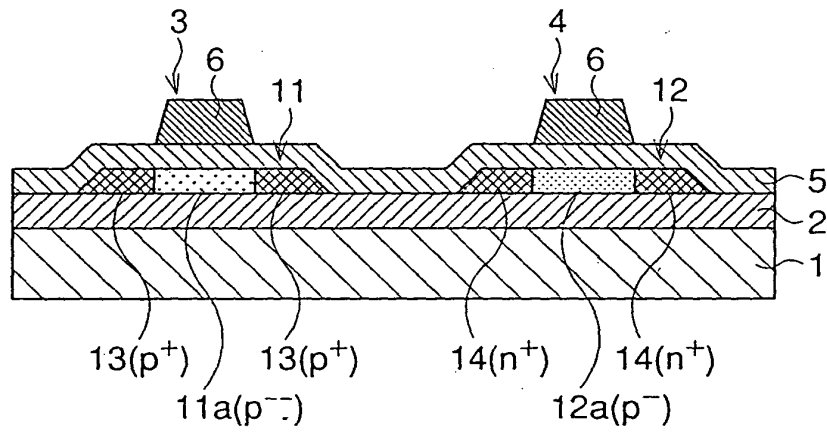


FIG. 5F

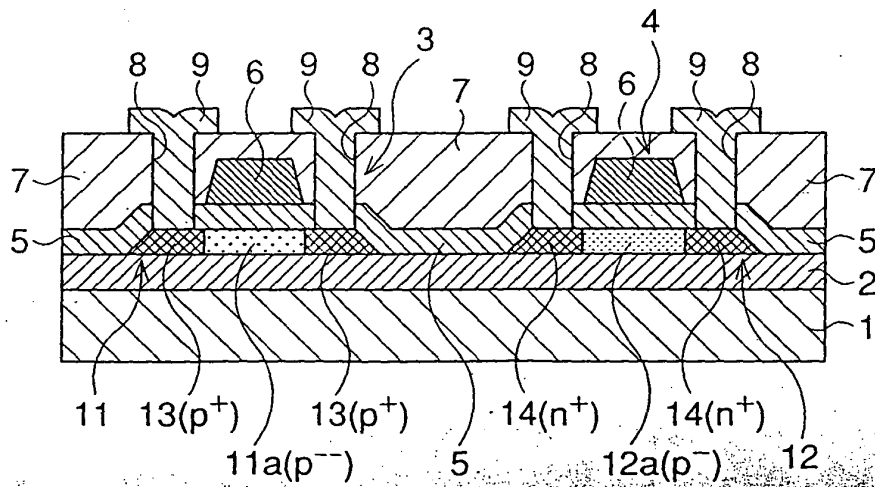


FIG. 6

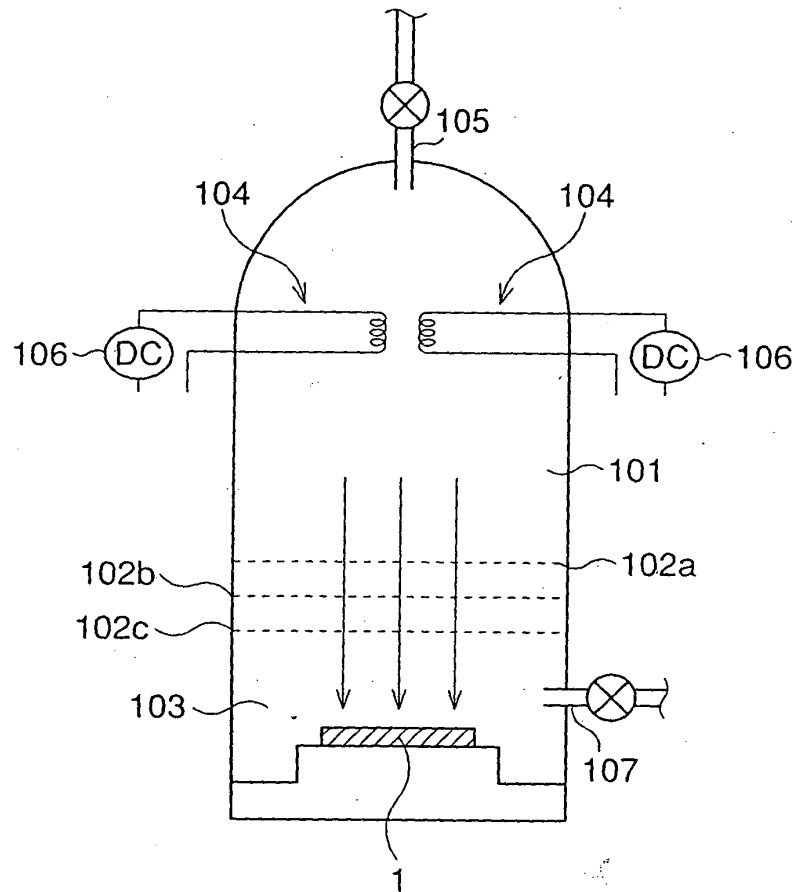


FIG. 7A

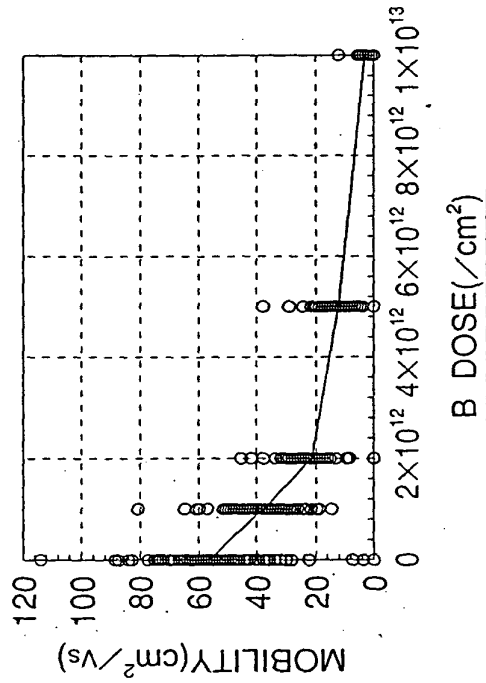


FIG. 7B

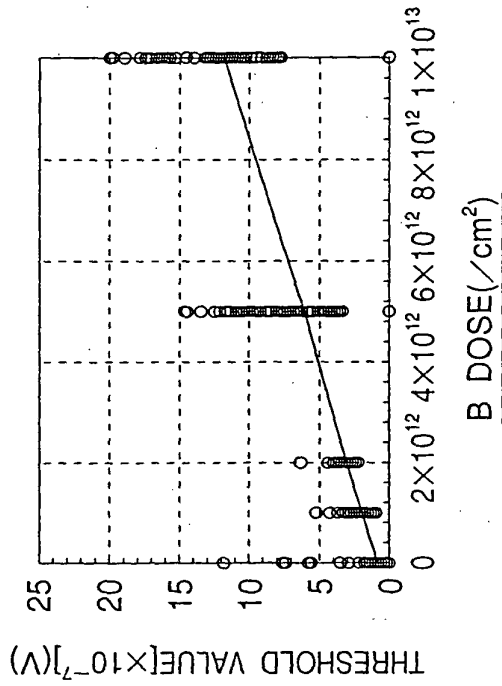


FIG. 7C

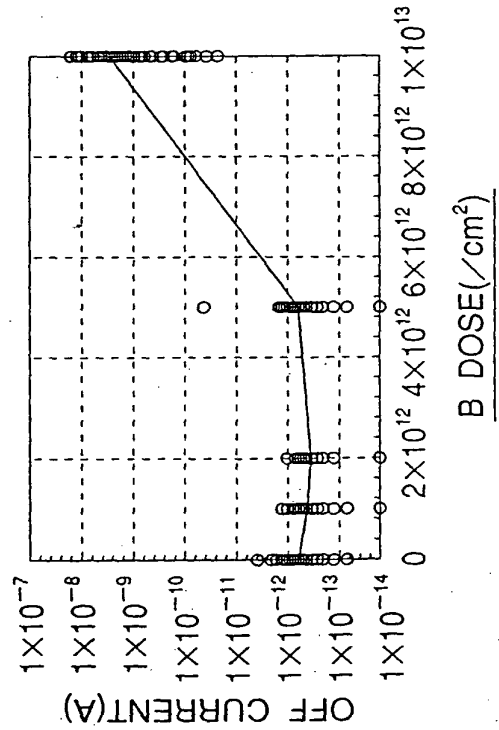


FIG. 7D

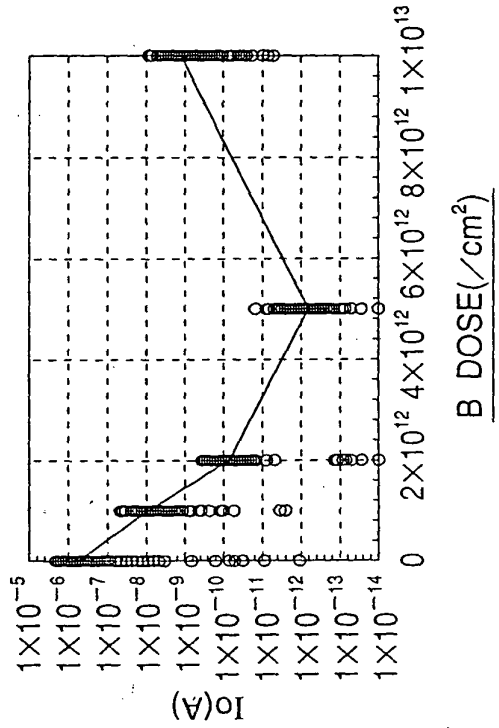




FIG. 8A

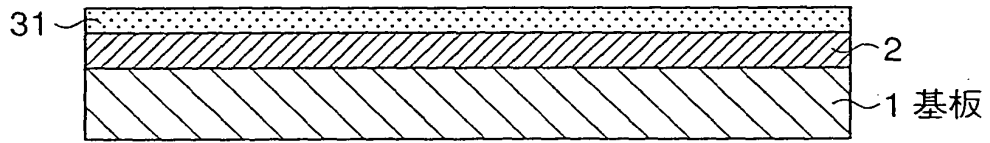


FIG. 8B

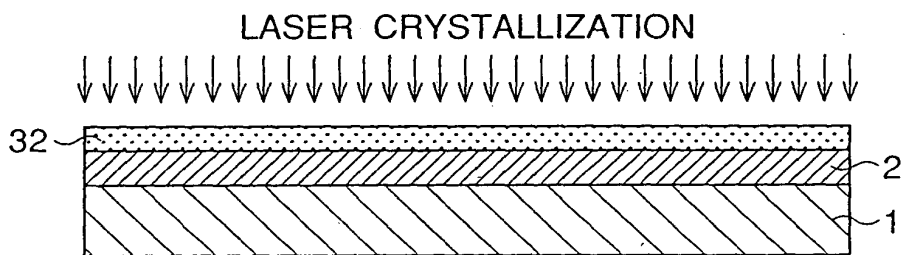


FIG. 8C

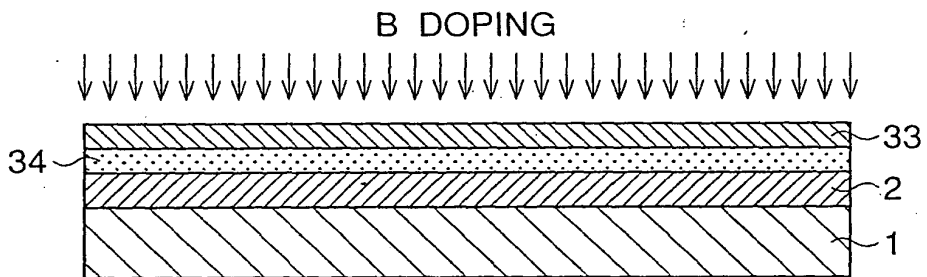


FIG. 8D

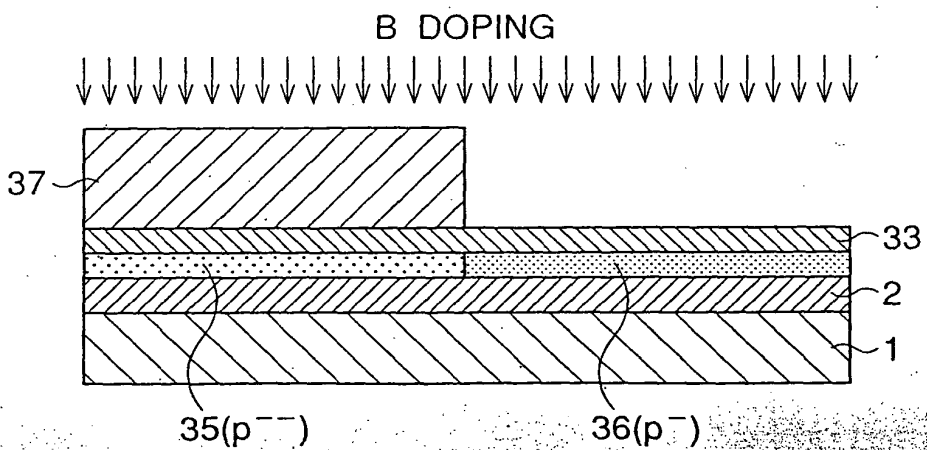


FIG. 9A

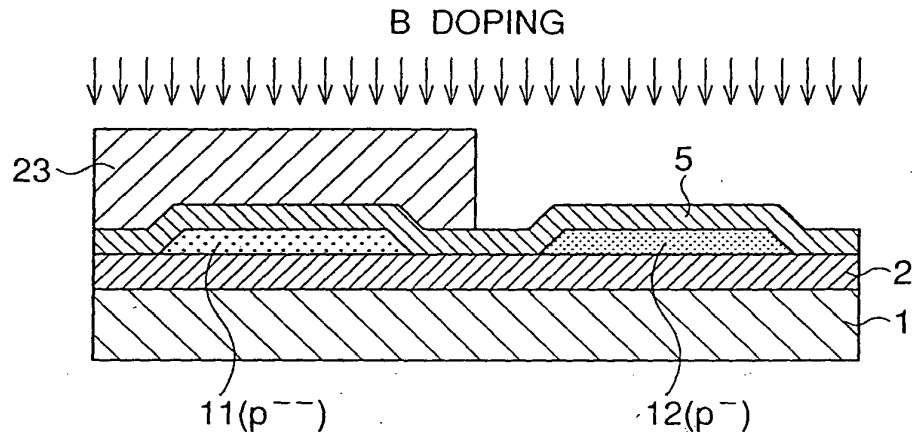


FIG. 9B

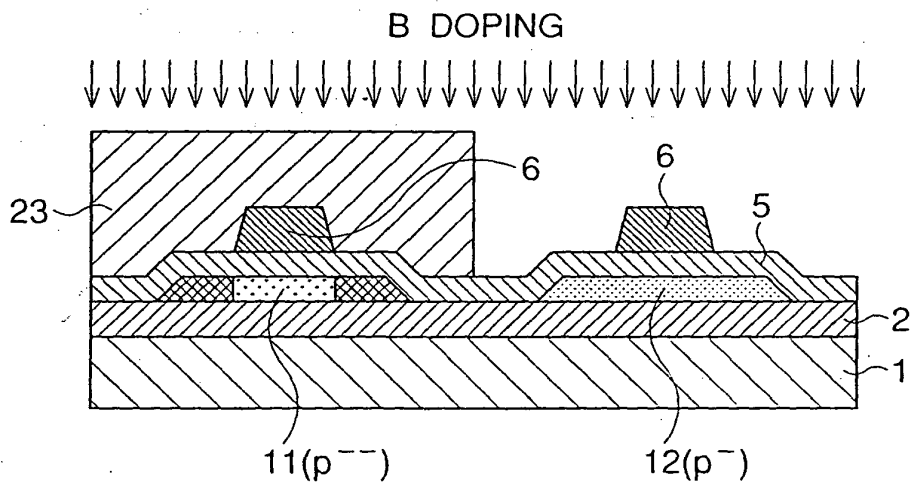


FIG. 10A

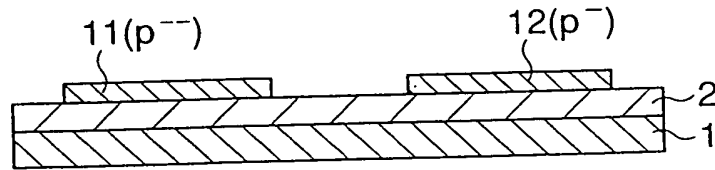


FIG. 10B

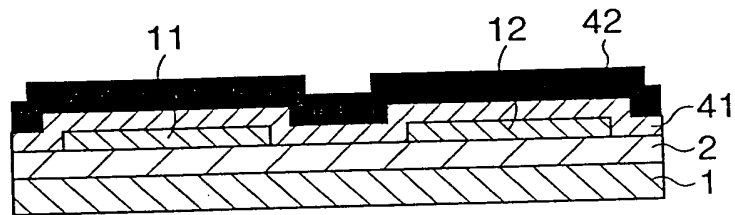


FIG. 10C

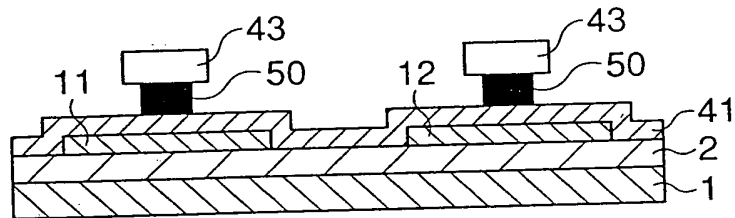


FIG. 10D

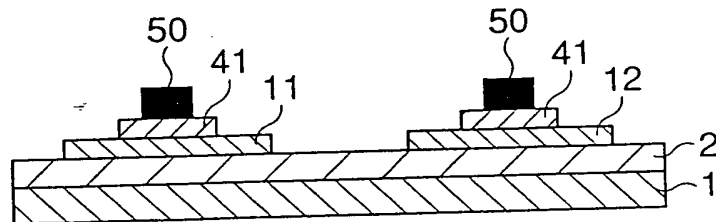


FIG. 10E

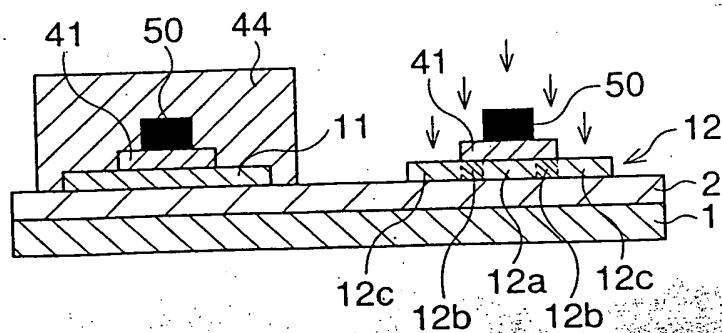


FIG. 10F

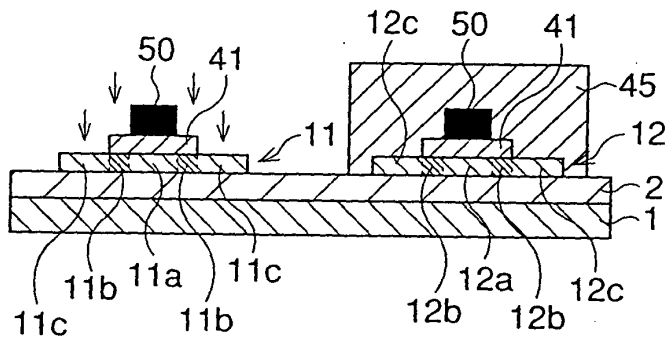


FIG. 10G

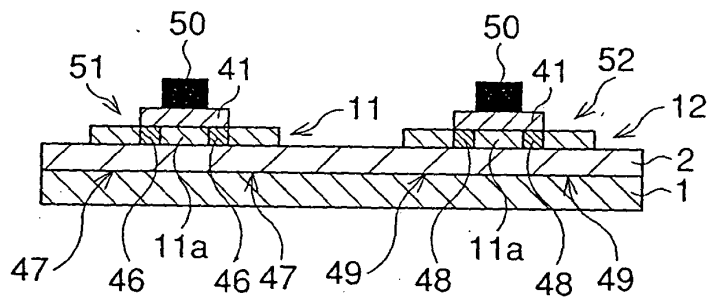


FIG. 10H

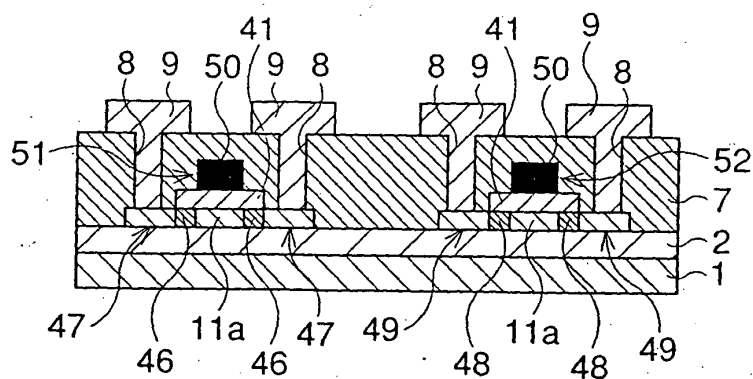


FIG. 11A

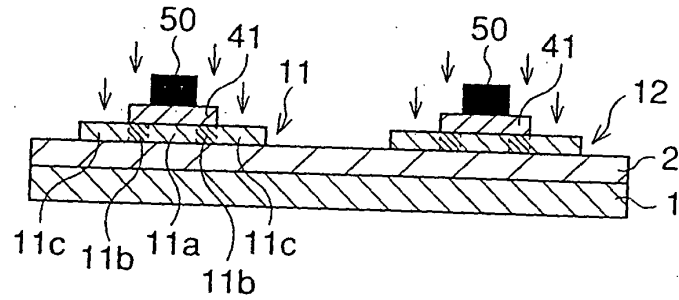


FIG. 11B

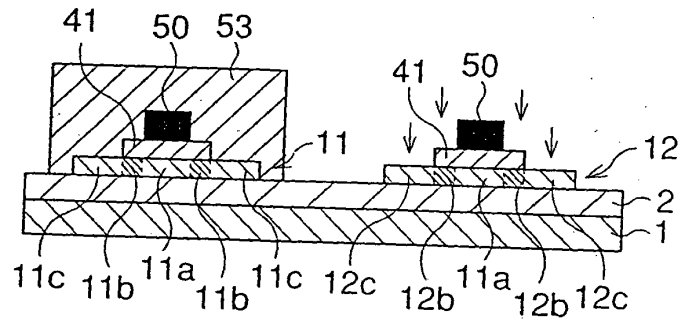


FIG. 11C

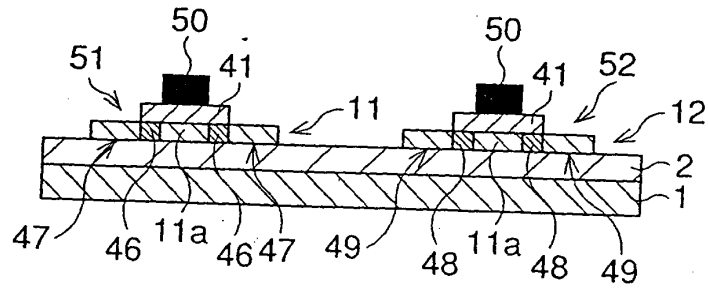


FIG. 11D

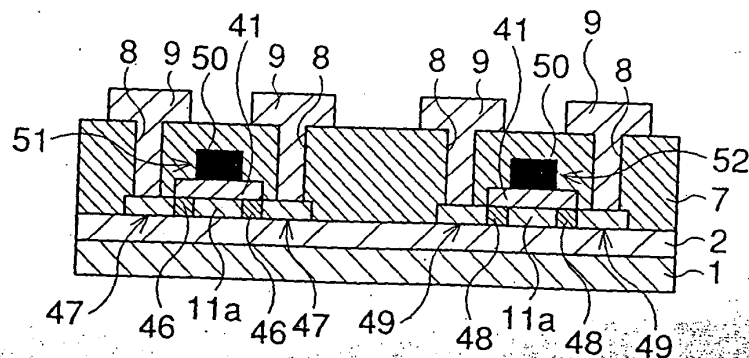


FIG. 12A

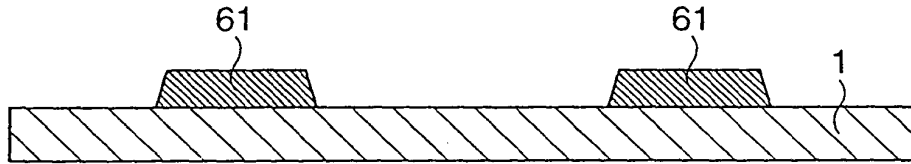


FIG. 12B

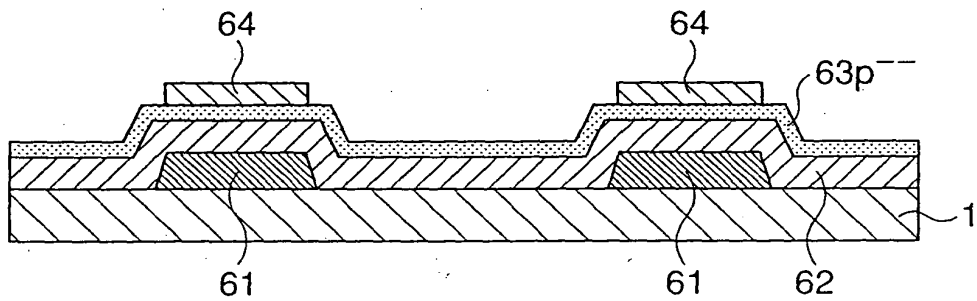


FIG. 12C

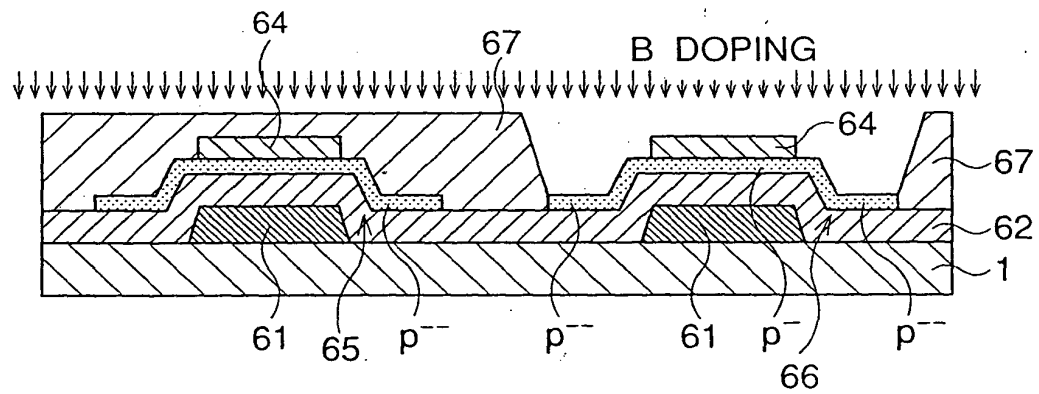


FIG. 12D

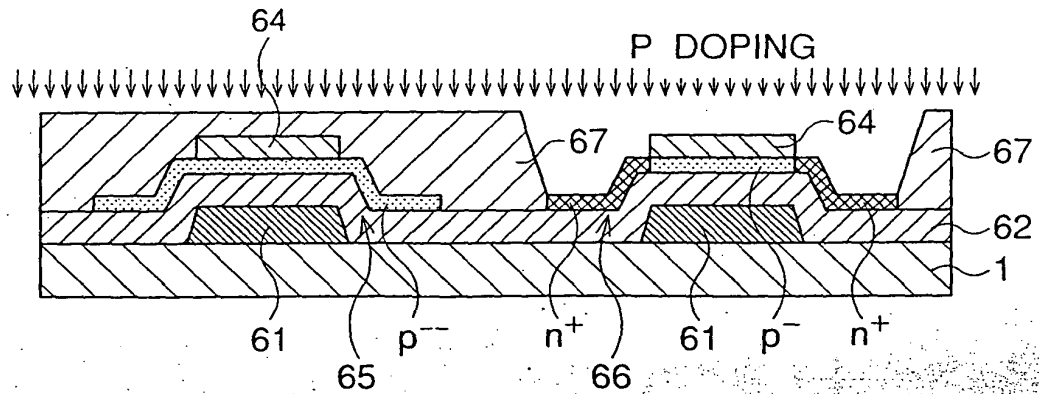


FIG. 12E

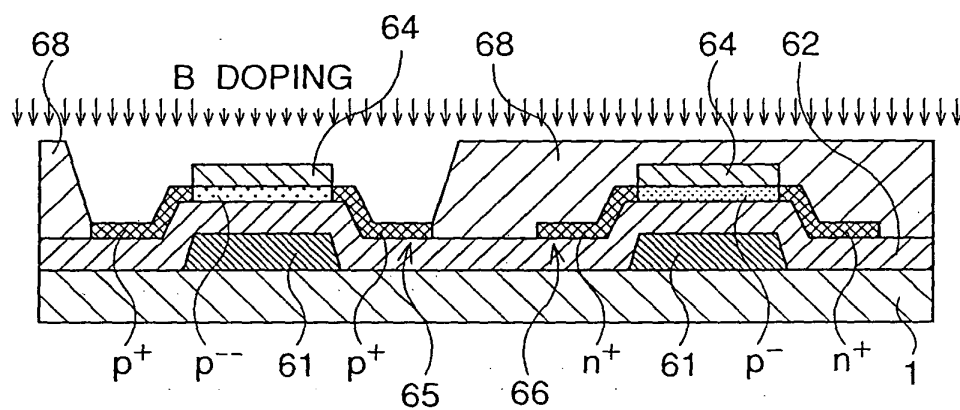


FIG. 12F

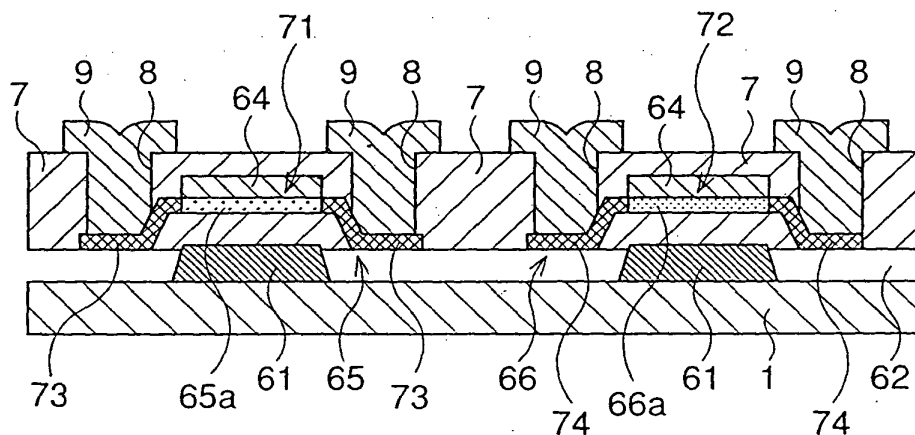


FIG. 13

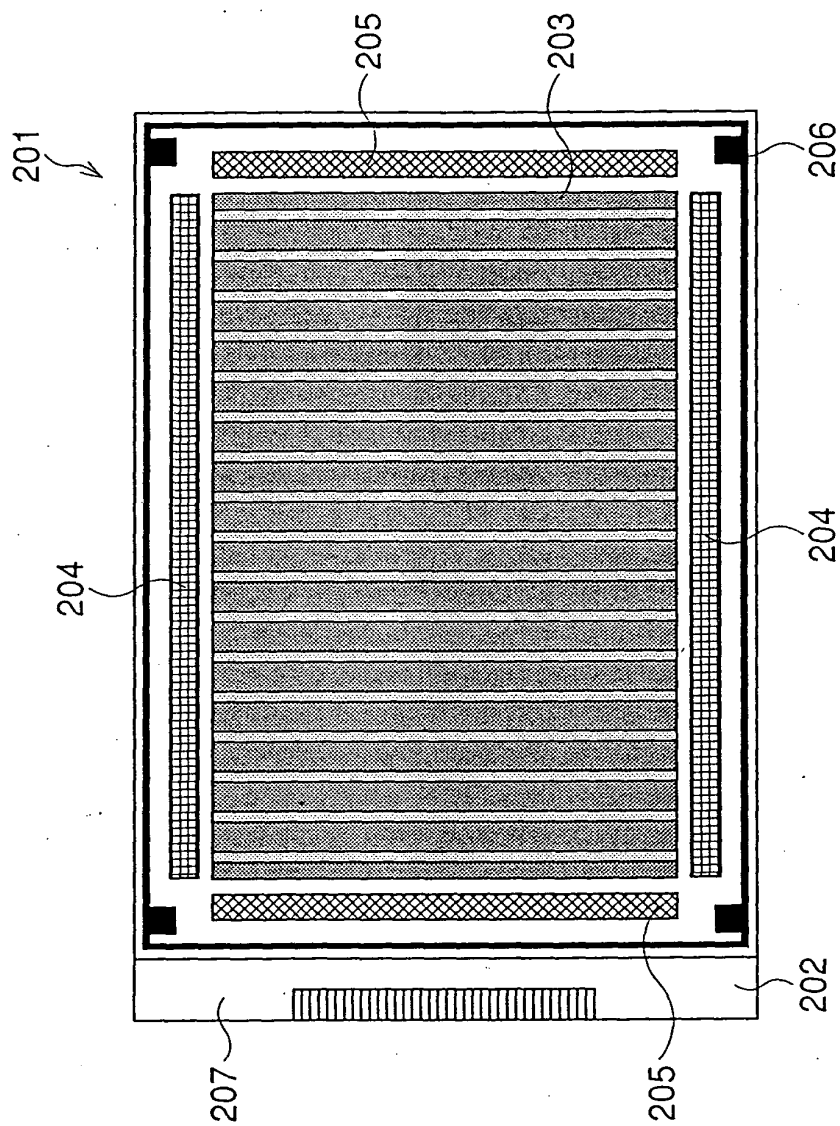




FIG. 14

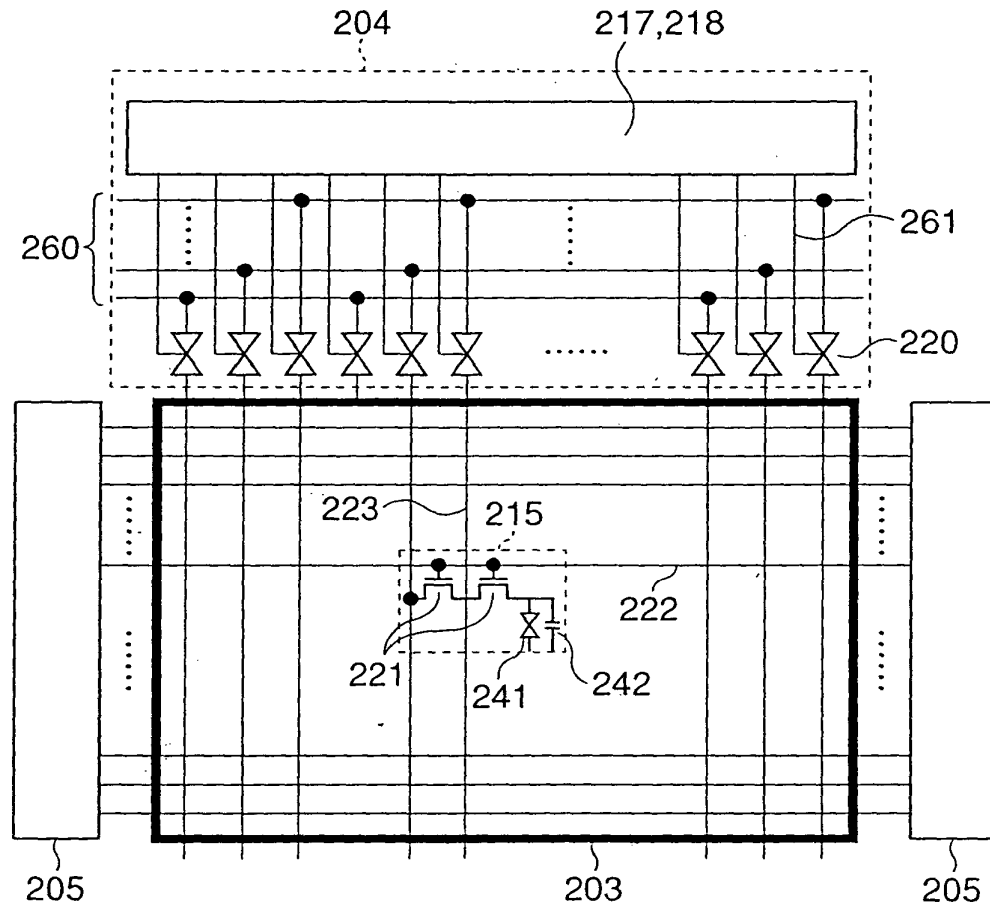


FIG. 15

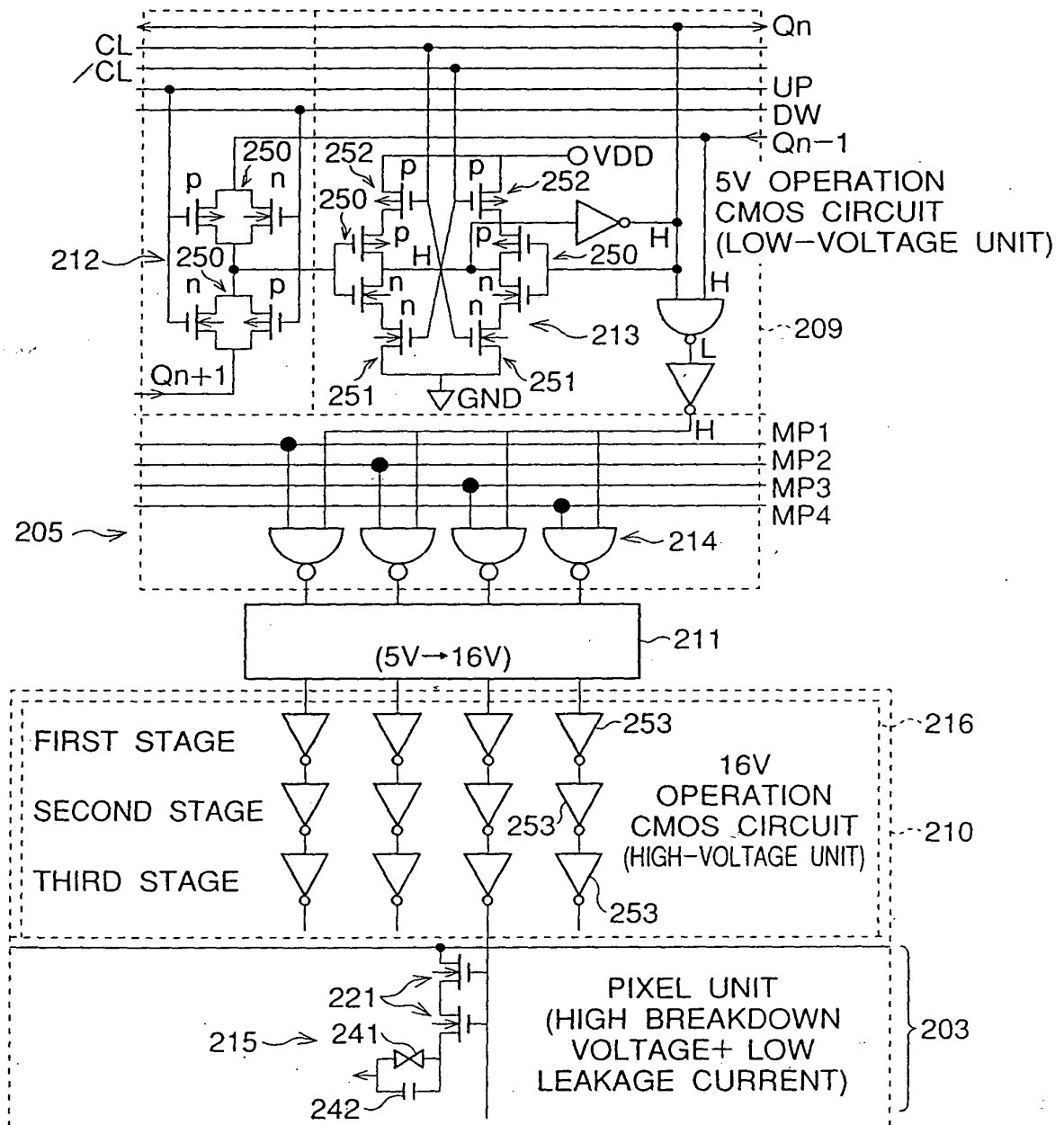


FIG. 16A

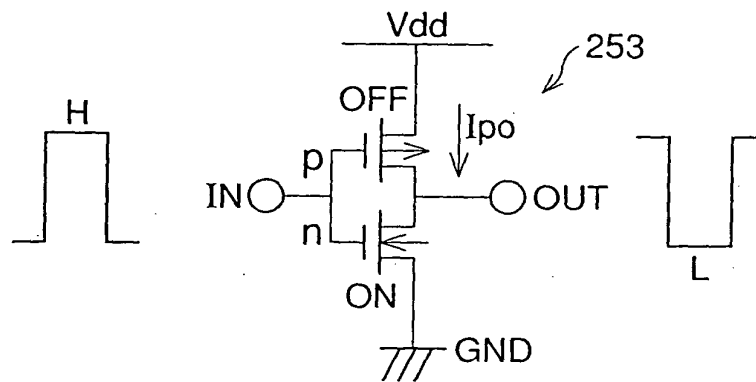


FIG. 16B

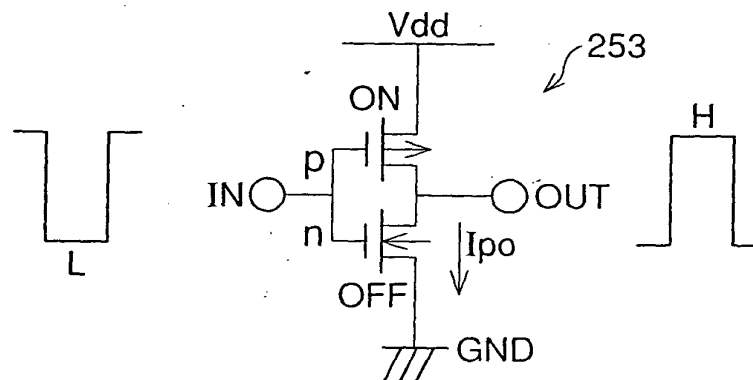


FIG. 17

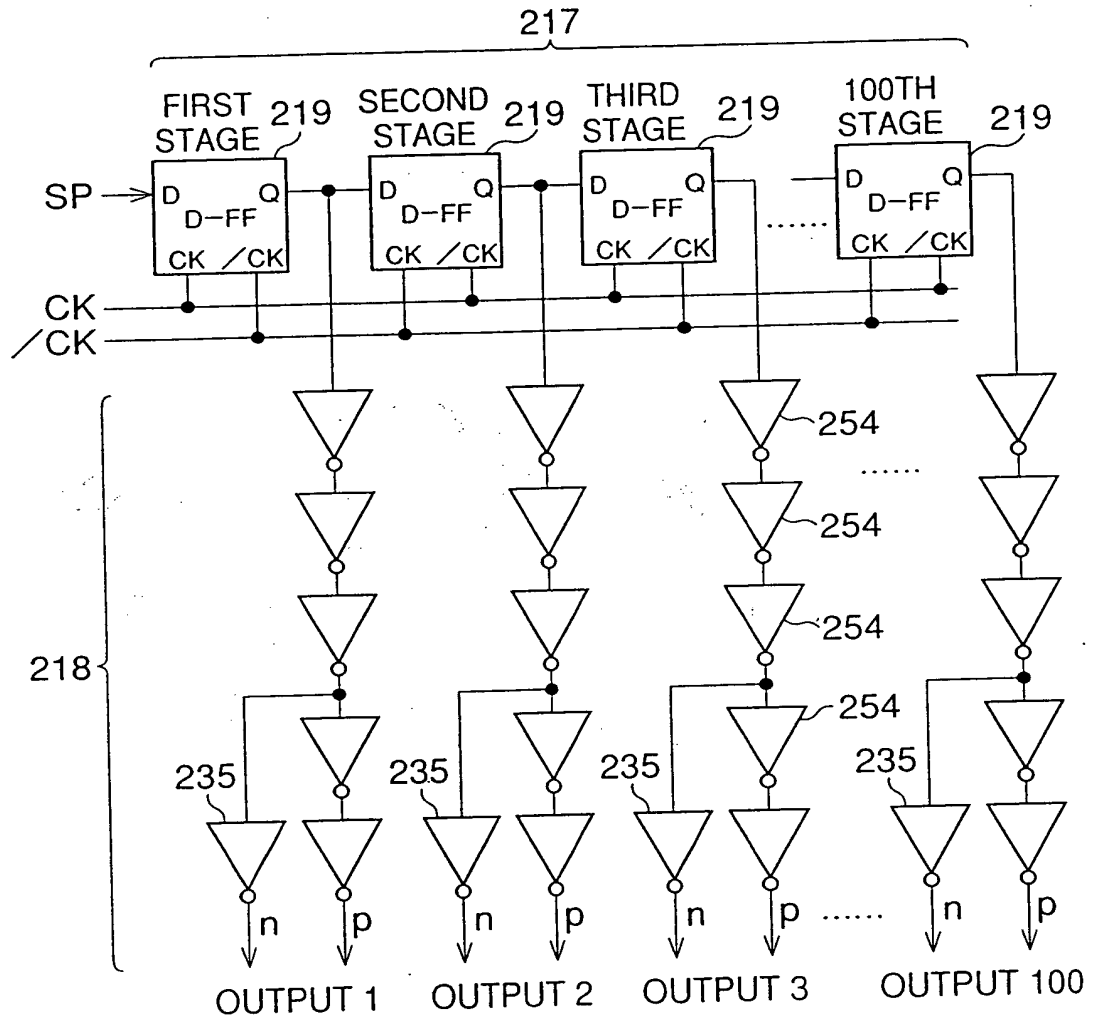


FIG. 18A

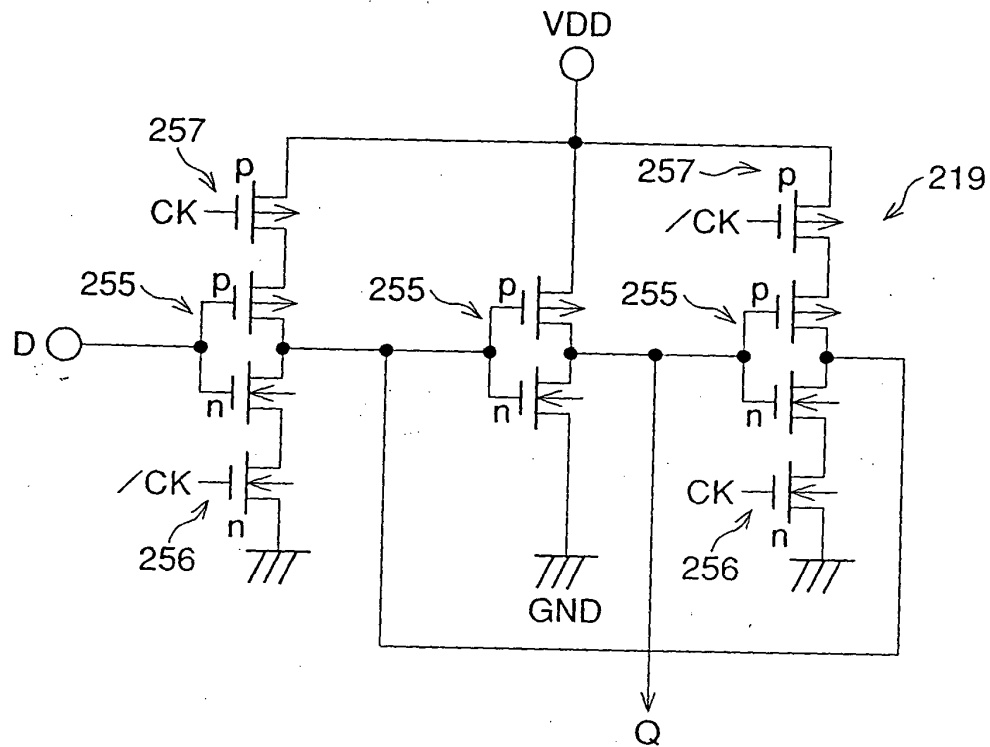


FIG. 18B

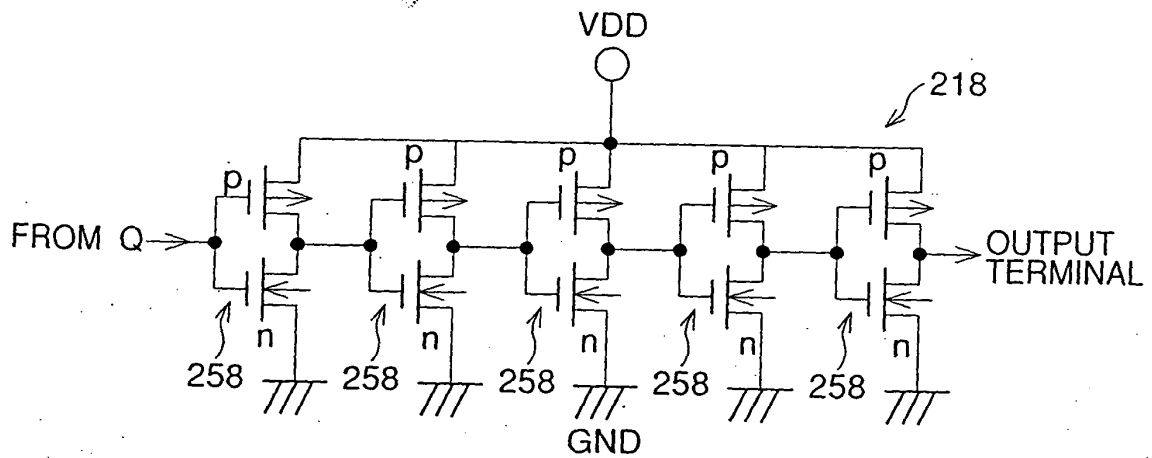


FIG. 19

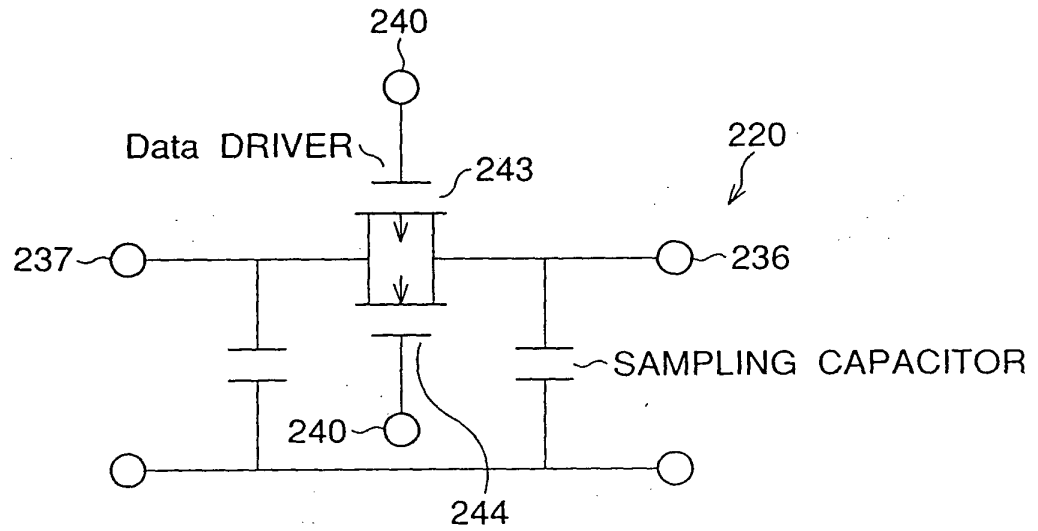


FIG. 20A

IMPURITIES B ARE ADDED TO  
 ENTIRE SURFACE DURING  
 PCVD a-Si FILM FORMATION.  
 (NON-SELECTIVELY IMPURITY DOPING)

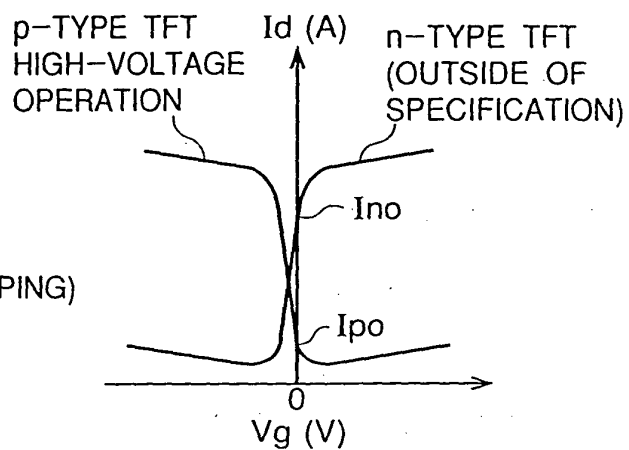


FIG. 20B

NON-SELECTIVELY DOPING (B)  
 n-AND p-TYPE TFTS (e.g., SHIFT  
 REGISTER) IN LOW-VOLTAGE  
 OPERATION UNIT

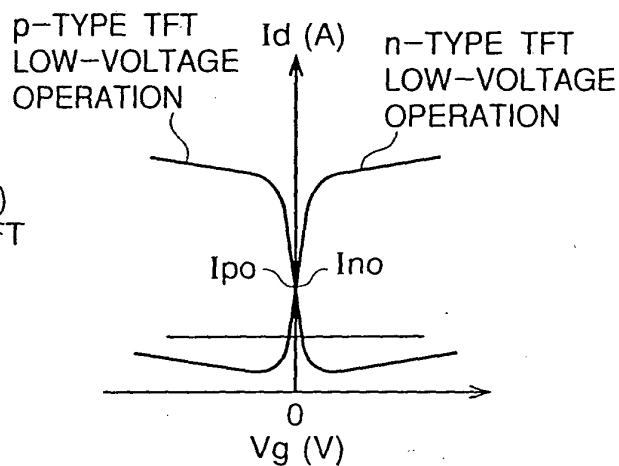


FIG. 21A

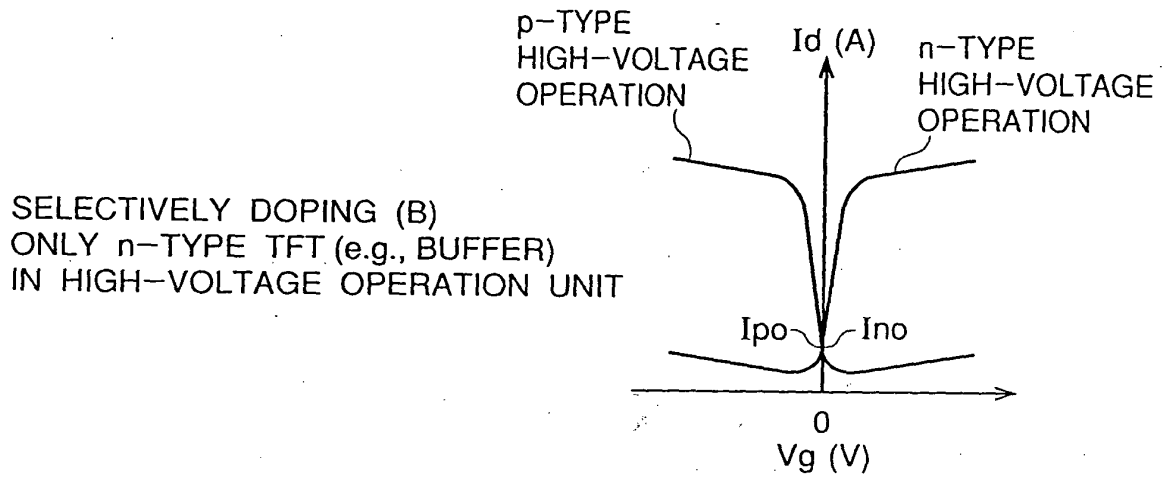


FIG. 21B

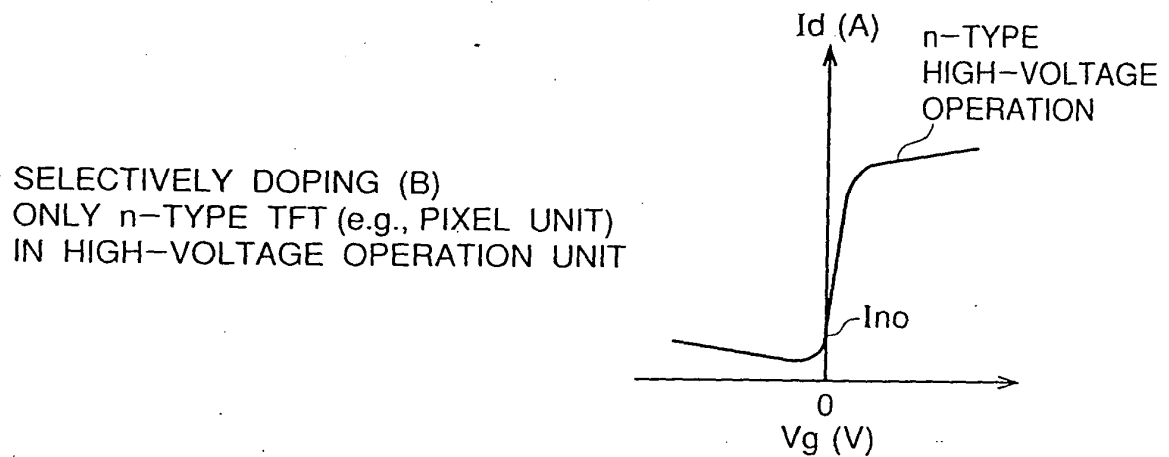




FIG. 22

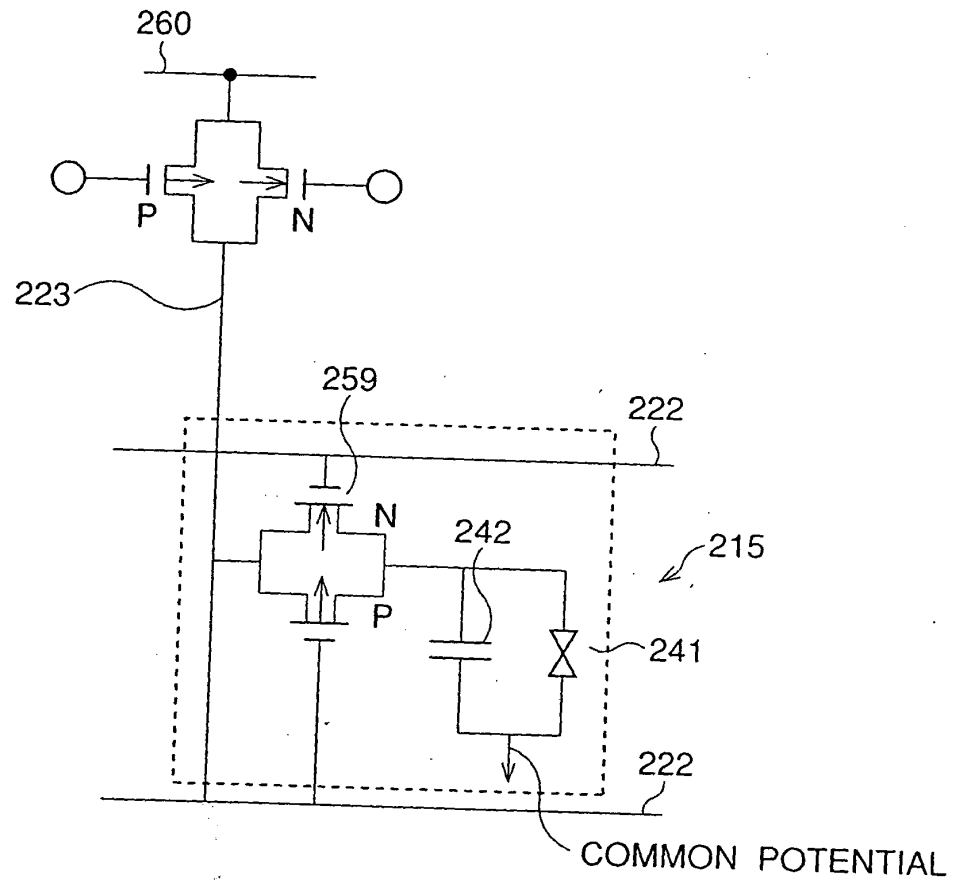


FIG. 23A

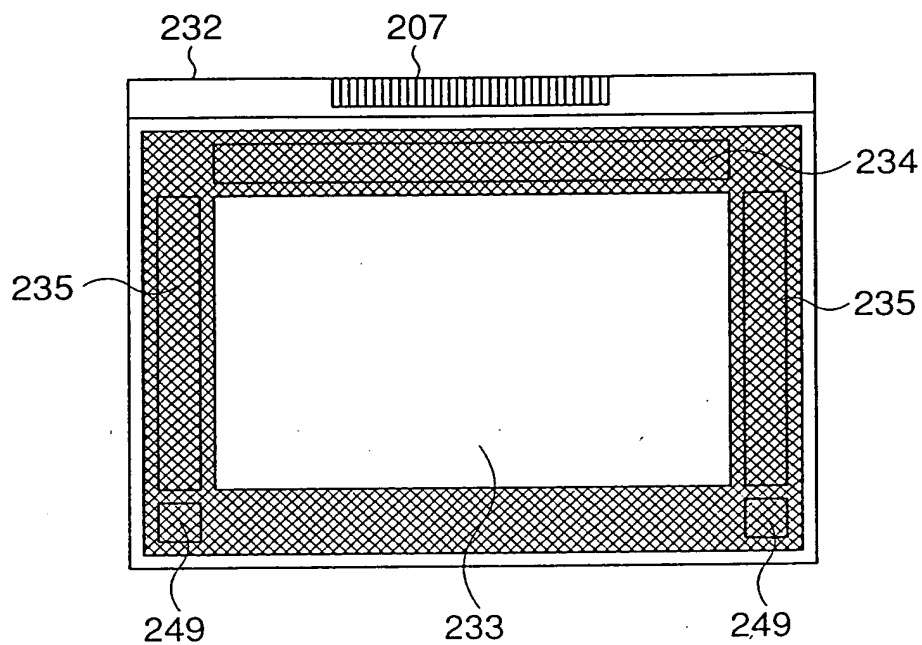


FIG. 23B

